ABSTRACT

A passenger transit car such as a rail car including a self-locking memory circuit for a tristate data bus having multiple bit lines. The self-locking circuit is located on a printed circuit board that is directly connected a mother board which, in turn, is directly connected to motors, solenoids and switches which couple considerably more electrical noise onto the data lines and the self-locking circuit than the electrical noise present in conventional environments for self-locking circuits. The circuit includes a non-inverting amplifier chip for connection to one of the bit lines and a resistor having a predetermined electrical resistance connected across the amplifier chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit to reduce the effects of electrical noise on the data bus. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below the upper and lower threshold levels of the self-locking circuit. The tristate data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.